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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,900	KO ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 30 December 2003 was fully considered by the examiner.

Drawings

3. The drawings were received on 30 December 2003. These drawings are deemed acceptable for examination.

Specification

4. The abstract of the disclosure is objected to because portions are not written very clearly. More specifically, lines 9-15 should be corrected to fix any obvious grammatical issues. A possible correction to these lines could include "N+1 number of unit tag tables, each having M number of registers and store information that the registers correspond to M number of word lines, each register stores each physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information".

Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities:

Just as described in paragraph four above, the description of the invention (per page 10 of the specification) is not written very clearly. A possible suggestion is provided above in paragraph four.

Appropriate correction is required.

Claim Objections

6. Claims 1-3 are objected to because of the following informalities:

As for claim 1, "a candidate information" recited on lines 6-7 (page 17) should be changed to "candidate information".

As for claim 2, line 24 (page 17) should be rewritten as follows "The semiconductor memory device as recited in claim 1, further comprising:"

As for claim 3, "tag table selection signal" should be changed to "a tag table selection signal", "all register" should be changed to "all registers", and "tag table" should be changed to "tag tables". These phrases can be found on lines 5, 19 and 20 (page 18) respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 3 recites, "to initialize each of the N+1 number of unit tag tables to each of the N+1 number of unit tag tables". The claim is not written sufficiently to enable one of ordinary skill in the art to carry out the claimed invention in light of this limitation. Furthermore, the specification fails to provide any additional support as to how a unit tag table can be initialized to itself.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, the phrase "to be stored data" as recited on lines 8-9 (page 17) renders the claim indefinite. More specifically, it would be unclear to one of ordinary skill in the art if the data is being stored in the word line, and if so, if the data is stored in the at least one or more candidate word line, or in one of the other M number of word lines. Additionally, the claim recites, "storing a store information that the registers corresponds to M number of word lines" in lines 16-17 (page 17). This phrase renders the claim indefinite as it unclear if the store

information is being stored in the resisters, the unit tag table, or the tag block itself, as recited in the claim.

As for claim 3, the phrase "selectively outputting one between the input logical cell block address and each of initialization signals" recited on lines 10-12 (page 18) renders the claim indefinite. More specifically, it is unclear the meaning of "one" as recited in this claim. It is unclear if the plurality of multiplexers are outputting an address, or an initialization signal, or selecting from one of the two. In either case, one of ordinary skill in the art would be unable to ascertain what exactly the plurality of first multiplexers is outputting as the claim is presently recited, and no further explanation to help clear up the ambiguity is provided in the specification.

As for claim 4, the step of "performing a normal operation of the semiconductor memory device by using the tag block" is recited on (line 27, page 18 through line 1, page 19). This limitation renders the claim indefinite for two reasons. First, one of ordinary skill in the art would be unable to ascertain the meaning of a "normal operation" of a semiconductor device. Furthermore, the specification fails to provide any additional description of what constitutes a "normal operation" of a memory device. Secondly, the step further recites performing said operation "by using the tag block". Again the limitation renders the claim indefinite, as one of ordinary skill in the art would be unable to ascertain how the block is being used to perform said operation.

Claims 2 and 5 inherit the deficiencies of claims 1 and 4 respectively, therefore they too stand rejected under 35 U.S.C. 112.

10. Claim 1 recites the limitation "the physical unit cell block address" in recited line 16 (page 17). There is insufficient antecedent basis for this limitation in the claim as a physical *unit* cell block address is not previously set forth in the claim, or the claim from which it depends. Likewise, there is insufficient antecedent basis for the limitation "the logical cell" recited in lines 18-19 (page 17) as a logical cell block is not previously set forth in the claim, or the claim from which it depends. Lastly, there is insufficient antecedent basis for the limitation "unit cell block addresses" recited in line 19 (page 17) as it is unclear if this limitation is referring back to the physical cell block address, or logical cell block address as recited in lines 10-12 of claim 1 (page 17).

Claim 3 recites the limitation "each of initialization activating signal" in recited lines 7-8 (page 18). There is insufficient antecedent basis for this limitation in the claim as activating signal is not previously set forth in the claim, or the claim from which it depends (only a selection signal). Likewise, there is insufficient antecedent basis for the limitation "the input logical cell block address" recited in line 11 (page 18) as an *input* logical cell block address is not previously set forth in the claim, or the claim from which it depends. Lastly, there is insufficient antecedent basis for the limitation "each of initialization signals" recited in lines 11-12 (page 18) as only one initialization signal is previously set forth in the claim (line 4, page 18).

Claim 5 recites the limitation "the N+1 number of unit tag tables" recited in line 5 (page 19). There is insufficient antecedent basis for this limitation in the claim as an

N+1 number of unit tag tables is not previously set forth in the claim, or the claim from which it depends. Likewise, there is insufficient antecedent basis for the limitation "each different logical unit cell block" recited in line 7 (page 19) as logical unit cell blocks are not previously set forth in the claim, or the claim from which it depends. Lastly, there is insufficient antecedent basis for the limitation "the N number of unit tag tables" recited in line 8 (page 19) as an N number of unit tag tables is not previously set forth in the claim, or the claim from which it depends.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Burger et al., hereinafter Burger (US Patent 6,557,080 B1) based on the Examiner's best understanding of the claims in light of the ambiguities set forth under sections 6-9 of this correspondence.

12. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Jarboe, JR. et al., hereinafter Jarboe (US PG Publication 2004/0153793 A1) based on the Examiner's best understanding of the claims in light of the ambiguities set forth under sections 5-8

of this correspondence. More specifically, Jarboe discusses initializing a tag block, and performing memory operations (i.e. read/write) based on the tag information – paragraph 0020, all lines.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jarboe as applied to claim 4 above, and in further view Yamaguchi et al., hereinafter Yamaguchi (US Patent 5,584,003).

Examiner asserts that Jarboe in further view of Yamaguchi renders claim 5 obvious based of the Examiner's best understanding of the claim in light of the ambiguities set forth under sections 8-9 of this correspondence. More specifically, Yamaguchi teaches a plurality of tables used to store information on cell blocks (i.e. addresses), and further selecting the tables in order to address the cell blocks (see col. 3, lines 51 through col. 4, lines 15.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Jarboe to further include Yamaguchi's control system into his own system for testing embedded memory. By doing so, Jarboe would benefit by improving address

conversion of the memory, thus resulting in higher processor performance as taught by Yamaguchi (col. 2, lines 37-47).

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

15. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claims 1-3 are provisionally rejected on the ground of nonstatutory double patenting over claim 42 of copending Application No.10/696,144. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

17. The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

Claim 1 of the instant application corresponds to (relevant sections of) claim 42 in the copending application as shown in the table below:

Claim 42: Copending Application 10/696,144	**Claim 1: Instant Application 10/749,900**
A memory device, comprising: a cell area having N+1 number of unit cell blocks, each including M number of word lines for responding to an inputted row	A *semiconductor* memory device, comprising: a cell area having N+1 number of unit cell blocks, each including M number of word lines;
a predetermined cell block table for storing information wherein at least more than one word line among the *(N+1) X M* number of the word lines is assigned as a predetermined restorable word line by using the information;	a predetermined cell block table for storing a *candidate* information representing at least more than one candidate word line among the M number of the word lines to be stored data; and
a tag block for sensing an input logical cell block address for designating a unit cell block to be accessed to converting the input logical cell block address into a physical cell block address for designating a unit cell block to be restored	a tag block for receiving a row address, sensing a logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information,
wherein the tag block further includes a cell block address decoder for outputting to one unit tag table selected in the N+1 number of the unit tag tables by decoding information wherein unit cell block of the N+1 number of the unit cell blocks has the predetermined word line corresponding to the word line selected by the local address outputted from the predetermined cell block table.	wherein the tag block includes: a N+1 number of unit tag tables, each having M number of registers and storing a store information that the registers corresponds to M number of word lines, each register storing each the physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information; and an *initialization unit for initializing the N+1 number of unit tag tables.*

18. Though not all elements of the instant application are present in the copending application with respect to claim 1-3, the claims are rendered obvious in further view of Berger based on the Examiner's best understanding of the claims in light of the ambiguities set forth under sections 6-9 of this correspondence.

It would have been obvious to one of ordinary skill in art at the time of the invention for Ahn et al., hereinafter Ahn (US PG Publication 2004/085835 A1) – i.e. copending application - to further include Burger's cache with dynamic control of sub-block fetching. By doing so Ahn would benefit from Burger's system by providing a dynamically changing fetch block size for updating the cache based on statistical data as to how well a previous fetch block size was utilized by the processor as taught by Burger (col. 2, lines 35-41), thereby improving the overall cache efficiency with respect to cache misses as taught by Burger in col. 1, lines 59-67.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Wang et al. (US Patent 6,697,909 B1) teaches a method and apparatus for performing data access and refresh operations in different sub-arrays of a DRAM cache memory.

Stracovsky et al. (US Patent 6,286,075 B1) teaches a method of speeding up access to a memory page using a number of M page tag registers to track a state of physical pages in a memory device having N memory banks were N is greater than M.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

2/20/01

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER